

**IN THE SPECIFICATION**

Please amend paragraph 9 of the specification as follows:

[p9] Additional advantages of this invention are 1) the behavioral model provided here captures driver delay, thereby allowing on-chip and off-chip timing to be merged into a seamless interface, 2) I/O current waveforms are readily available for on-chip power grid integrity analysis, and 3) signal integrity analysis at the chip level is available without the need of procuring other software. Furthermore, the behavioral model provided by this invention can be used to enhance other applications that currently perform package noise analysis using full netlist models which greatly limits the cross sectional size it can analyze at one time. These advantages enable these models, herein referred to as "BIO" (Behavioral I/O) models, to form a seamless interface between on-chip and off-chip timing. They can also provide accurate rail current waveforms for power grid analysis tools and I/O placement tools. Because BIO models have the ability to handle ground bounce and power supply collapse, they can also be used in signal integrity tools.